Code No: **P41051** **R10** **Set No. 1**

**IV B.Tech I Semester Supplementary Examinations, March/April - 2016**

# COMPUTER ARCHITECTURE

**(Computer Science and Engineering)**

**Time: 3 hours** **Max. Marks: 75**

**Answer any FIVE Questions**
**All Questions carry equal marks**
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|---|---|---|---|
| 1 | a) | Briefly explain the program flow mechanisms and Compare. | [8] |
| | b) | Draw and Explain the architecture of Vector Super computers. | [7] |
| 2 | | What is meant by Cache optimization? Briefly explain the Cache optimization techniques? | [15] |
| 3 | a) | Briefly explain the hierarchical memory technology with neat diagram? | [8] |
| | b) | Differentiate between CISC and RISC processors | [7] |
| 4 | | How does a collision occur in nonlinear pipeline processors? Briefly Explain the collision free scheduling of events in non linear pipeline systems | [15] |
| 5 | a | Explain about the different types of vector instructions | [8] |
| | b | What is Hot Spot Problem? Briefly explain it with an example? | [7] |
| 6 | a) | What is Cache coherence problem? Explain any Cache coherence protocol | [8] |
| | b) | What is deadlock? Explain about deadlock virtual channel | [7] |
| 7 | a) | Draw and explain CM-2 Architecture. | [8] |
| | b) | Explain the Intercommunications in the Synchronized MIMD systems. | [7] |
| 8 | | Briefly explain the forms of parallelism? Compare them. | [15] |